WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a plurality of word lines, a plurality of data lines, and a plurality of DRAM memory cells;

a plurality of sense amplifiers coupled to said plurality of data lines and each receiving operating voltage from first and second nodes;

a first line connected to said first nodes;

a second line connected to said second nodes;

a first drive for coupling said first line with a first potential; and

a second drive for coupling said second line with a second potential;

wherein said first drive sets up a connection between the first potential and said first line at a first impedance in a first operation mode and a connection between the first potential and said first line at a second impedance higher than the first impedance in a second operation mode,

wherein said second drive sets up a connection between the second potential and said second line at a third impedance in the first operation mode and a connection between the second potential and said second line at a

fourth impedance higher than the third impedance in the second operation mode,

wherein a change from the first operation mode to the second operation mode occurs after a first time from a row active command.

2. The semiconductor device according to claim 1,

wherein said first drive includes a first switch and a second switch disposed in parallel between said first line and the first potential, and

wherein said second drive includes a third switch and a fourth switch disposed in parallel between said second line and the second potential.

3. The semiconductor device according to claim 2,

wherein said first switch is selectively put into conduction in the first operation mode, and said second switch is selectively turned on in the second operation mode,

wherein a conductance of said first switch is larger than a conductance of said second switch,

wherein said third switch is selectively put into

conduction in the first operation mode, and said fourth switch is selectively turned on in the second operation mode, and

wherein a conductance of said third switch is larger than a conductance of said fourth switch.

4. The semiconductor device according to claim 2,

wherein each of said plurality of sense amplifiers includes an NMISFET pair arranged in a cross-coupled form and a PMISFET pair arranged in a cross-coupled form.

5. The semiconductor device according to claim 2,

wherein the second operation mode ends when a precharge command is issued.

6. A semiconductor device comprising:

a plurality of word lines, a plurality of data lines, and a plurality of DRAM memory cells;

a plurality of sense amplifiers coupled to said plurality of data lines and each receiving operating voltage from first and second nodes;

a first line connected to said first nodes;

a second line connected to said second nodes;

first drive means for coupling said first line with a first potential; and

second drive means for coupling said second line with a second potential;

wherein each of said plurality of sense amplifiers includes a first NMISFET pair arranged in a cross-coupled form and a second PMISFET pair arranged in a cross-coupled form,

wherein said first drive means sets up a connection between the first potential and said first line at a first impedance in a first operation mode and a connection between the first potential and said first line at a second impedance higher than the first impedance in a second operation mode,

wherein said second drive means sets up a connection between the second potential and said second line at a third impedance in the first operation mode and a connection between the second potential and said second line at a fourth impedance higher than the third impedance in the second operation mode,

wherein said first drive means includes a first NMISFET and a first PMISFET disposed in parallel between said first line and the first potential, and

wherein said second drive means includes a second NMISFET and a second PMISFET disposed in parallel between said second line and the second potential.

7. The semiconductor device according to claim 6,

wherein a change from the first operation mode to the second operation mode occurs after a first time from a row active command.

8. The semiconductor device according to claim 7,

wherein the second operation mode ends when a precharge command is issued.

9. A semiconductor device comprising:

a plurality of word lines, a plurality of data lines, and a plurality of DRAM memory cells;

a plurality of sense amplifiers coupled to said plurality of data lines and each receiving operating voltage from first and second nodes;

a first line connected to said first nodes;

a second line connected to said second nodes;

first device means for coupling said first line with a first potential; and

second drive means for coupling said second line with a second potential;

wherein each of said plurality of sense amplifiers includes a first NMISFET pair arranged in a cross-coupled form and a second PMISFET pair arranged in a cross-coupled form,

wherein said first drive means sets up a connection between the first potential and said first line at a first impedance in a first operation mode and a connection between the first potential and said first line at a second impedance higher than the first impedance in a second operation mode,

wherein said second drive means sets up a connection between the second potential and said source line at a third impedance in the first operation mode and a connection between the second potential and said second line at a fourth impedance higher than the third impedance in the second operation mode,

wherein said first drive means includes a first PMISFET having its source/drain path between said first line and the first potential;

wherein said second drive means includes a first NMISFET having its source/drain path between said first line and the first potential,

wherein the gate voltage of said first PMISFET in said second operation is controlled between the gate voltage of said first PMISFET in said first operation and said first potential, and

wherein the gate voltage of said first NMISFET in said second operation is controlled between the gate voltage of said first NMISFET in said first operation and said second potential.

10. The semiconductor device according to claim 9,

wherein a change from the first operation mode to the second operation mode occurs after a first time from a row active command.

11. The semiconductor device according to claim 10,

wherein the second operation mode ends when a precharge command is issued.

12. A semiconductor device comprising:

a plurality of word lines, a plurality of data lines, and a plurality of DRAM memory cells;

a plurality of sense amplifiers coupled to said plurality of data lines and each receiving operating voltage from first and second nodes;

a first line connected to said first nodes;

a second line connected to said second nodes;

first drive means coupled to said first line;

second drive means coupled to said second line;

wherein each of said plurality of sense amplifiers includes a NMISFET pair arranged in a cross-coupled form and a PMISFET pair arranged in a cross-coupled form,

wherein said first drive means sets said first line to have a first potential, a second potential, a third potential between a row active command and a precharge command,

wherein said second drive means sets said second line to have a fourth potential, a fifth potential, a sixth potential between said row active command and said precharge command,

wherein after said row active command is issued, said first drive means drives said first line to said first potential and then to said second potential, and before

said precharge command is issued, said first drive means drives said first line from said second potential to said third potential,

wherein said second potential is lower than said first potential, and is higher than said third potential,

wherein after said row active command is issued, said second drive means drives said second line to said fourth potential and then to said fifth potential, and before said precharge command is issued, said second drive means drives said second line from said fifth potential to said sixth potential, and

wherein said fifth potential is higher than said fourth potential, and is lower than said sixth potential.

13. The semiconductor device according to claim 12,

wherein said first drive means drives said first line to said first potential in response to a first signal, and drives said first line from said second potential to said third potential in response to a second signal.

14. The semiconductor device according to claim 13,

wherein said second drive means drives said second line to said fourth potential in response to a third

signal, and drives said second line from said fifth potential to said sixth potential in response to a fourth signal.

15. The semiconductor device according to claim 14,

wherein said first line is coupled to said PMISFET pairs, and

wherein said second line is coupled to said NMISFET pairs.

16. The semiconductor device according to claim 14,

wherein a voltage level of said third signal is the same as a voltage level of a word line when selected.

17. The semiconductor device according to claim 15,

wherein said first drive means includes a first PMISFET having its source/drain path between said first line and the second potential,

wherein said second drive means includes a first NMISFET having its source/drain path between said second line and the fifth potential,

wherein a gate of said first PMISFET receives said second signal, and

wherein a gate of said first NMISFET receives said fourth signal.